have enclosed pages from two textbooks, both of which show the source connection which is part of the transistor. The circuit of the present invention includes the arrangement of transistors shown in the drawings and described in the specification. This arrangement includes the bulk diodes between the source and the body. It appears that the Office Action assumes different positions for the source and drain of the transistors, which could be leading to the confusion about the present invention.

The Office Action also suggests that the diodes in the figures are reversed. For example, the Office Action states that the polarity of diode D4 should be reversed "because current can only flow from the body of M4 to M4's N type source." However, the source electrode is connected to the body (which is what is illustrated by the bulk electrodes in Fig. 3) and current flows from the body to the N type drain. As illustrated in the attached pages from the textbooks, the current flow for an N type MOSFET is drawn from the source to the body, and for a P type MOSFET the current is drawn from the body to the source. Therefore, the figures and the description in the specification are in conformance with standard practice and properly describe the arrangement of the transistors in the circuit of the present invention.

Applicants have amended claims 3, 5, 6, 13, 14, 21, and 22 to correct the indefinite language recited in the Office Action. In particular, with respect to claims 3 and 5, the claim language has been changed to refer to the arrangement of the transistors and corresponding bulk diodes so that the necessary bridge structures are formed. Accordingly, the rejection under 35 U.S.C. § 112, second paragraph, has been overcome and should be withdrawn.

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Applicants respectfully traverse the rejection of the claims as being anticipated by or obvious in view of Matsumura or Okada. Matsumura and Okada both disclose substrate bias generators having similar structures. The structures in both references include four p type transistors (13-16 in Matsumura; T1, T2, TD1, TD2 in Okada) in a single N well. The transistors are connected so as to bias the substrate. The Office Action suggests that the substrate in these references operates as charge accumulation capacitor recited in the claims. However, although the reference structures include four transistors, they are connected and do not operate in the same manner as the structures recited in the claims of the present invention. In both references, two of the transistors have their gate and source connected (13, 14, TD1, and TD2). These transistors do not operate as switches in providing an increased voltage, but operate as rectifiers (see column 3, lines 59-60 in Okada and column 3, line 59 to column 4, line 12 of Matsumura). This structure has reduced efficiency as a voltage doubler. Also, in Matsumura, additional circuitry must be added to bias the transistors 13 and 14.

On the other hand, the present invention discloses a structure with two p type MOS transistors and two n type MOS transistors. The different types of transistors allows all of the transistors to operate as switches, and allows the circuit to have a high efficiency. The connections between the transistors operates for form two bridges, one with the conduction paths of the transistors and one with the bulk diodes of the transistors. The structures shown in Matsumura and Okada do not include the same connections so that the two bridges are not formed.

Thus, claim 1 recites a voltage doubler which includes, in part, two inverters connected together in a loop to form a flip-flop. Neither of the cited references teaches or suggests two inverters connected in the manner recited in claim 1. Claim 2 depends from claim 1 and recites that the inverters include MOS transistors and corresponding bulk terminals of the transistors connected to form a one-way conduction path. Neither of the references teaches or suggest two inverters with MOS transistors connected to form the one-way conduction path as recited in claim 2. Rather, the references recite two transistors operating as switches and two transistors operating as rectifiers. The references do not teach or suggest anything about the bulk terminals of the transistors. Accordingly, claims 1 and 2 patentably distinguishes over the cited art and are in condition for allowance.

Similarly, claim 3 recites a voltage doubler which includes a bridge formed of four transistors and corresponding bulk diodes of the transistors. The transistors and diodes are arranged to have certain reiterated conduction paths. The cited references do not teach or suggest the bridge circuit recited in claim 3. In fact, neither reference teaches or suggests anything about the connections between the bulk diodes of the transistors in a voltage doubling circuit. Thus, claim 3 patentably distinguishes over the cited art and is in condition for allowance. Claim 4 depends from claim 3 and is allowable for at least the same reasons.

Claim 6 also recites a voltage booster having a charging section with a bridge of controlled switches. Neither of the cited references teaches or suggests such a charging section. As discussed above, Matsumura and Okada only have two controlled switches. The other

transistors operate as rectifiers, not as controlled switches. Therefore, neither reference teaches or suggests a bridge structure of controlled switches. Accordingly, claim 6 patentably distinguishes over the cited art. Claims 7-11 depend from claim 6 and are allowable for at least the same reasons.

Similarly, claim 13 recites a memory device operable at a low voltage which includes at least one charging section as recited in claim 6. Claim 14 also includes the at least one charging section as recited in claim 6. For the same reasons, claims 13 and 14 patentably distinguishes over the cited art and is in condition for allowance.

Claim 19 recites a voltage multiplier including at least one bridge circuit as part of a multiplying means. The cited art does not teach or suggest such a structure. Claims 16-18 and 20-22 depend from claim 19 and are allowable for at least the same reasons. Furthermore, claim 20 recites a plurality of bridge circuits connected to corresponding first and second charge transfer condensers. Neither Matsumura nor Okada teaches or suggest multiple bridge circuits with separate charge transfer condensers. Claims 21 and 22 recite that the bridge circuits include four diodes (the bulk diodes) and four transistors having a structure allowing certain conduction paths. The cited art does not teach or suggest a bridge circuit including diodes and transistors arranged as recited in claims 20 and 21. Accordingly, claims 16-22 are in condition for allowance.

Finally, claims 24 and 25 relate to methods for generating an output voltage by applying certain input voltages and control voltages to one or more bridge circuits. The cited art does not

teach or suggest applying voltages to bridge circuits as recited in claims 24 and 25.

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,

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